Amendments To The Claims:

This listing of the claims will replace all prior versions and listings of claims for this application:

Listing of Claims:

1. (Previously presented) A diode, said diode comprising:

an isolation region formed in a substrate;

a first doped active layer of a first conductivity type formed in said substrate, wherein said doped active layer is spaced apart from said isolation region;

a second doped active layer of a second conductivity type in contact with said first doped active layer, the contact of said first and second active layers forming a p-n junction; and

a third doped region formed in said second doped active layer beneath said isolation region.

2. (Original) The diode according to claim 1, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

3. (Original) The diode according to claim 1, wherein said isolation region is a field oxide region formed by the Local Oxidation of Silicon process.

4. (Original) The diode according to claim 1, wherein said isolation region is a field oxide region formed by the Shallow Trench Isolation process.

5. (Original) The diode according to claim 1, wherein said first doped active layer is spaced from said isolation region by from about 0.05 μm to about 1.0 μm.

6. (Original) The diode according to claim 5, wherein said first doped active layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

7. (Previously presented) The diode according to claim 6, wherein said first doped active layer is spaced from said isolation region by about 0.2 μm to 0.7 μm.

Claim 8 (Canceled).

9. (Currently amended) The diode according to claim 1, wherein said third doped region is spaced away from ~~the~~ an edge of said isolation region at a surface of said substrate.

10. (Previously presented) The diode according to claim 1, wherein said third doped region is a p-type region.

11. (Original) The diode according to claim 1, wherein said first doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

12. (Original) The diode according to claim 11, wherein said first doped active layer is doped with phosphorous.

13. (Original) The diode according to claim 11, wherein said first doped active layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

14. (Previously presented) The diode according to claim 1, wherein said third doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

15. (Original) The diode according to claim 1, wherein said first doped active layer is an n-type active layer and said second doped active layer is a p-well.

16. (Previously presented) The diode according to claim 1, further comprising a fourth doped active layer at least partially within said first doped active layer.

17. (Currently amended) The diode according to claim 16, wherein said fourth doped active layer is spaced away from ~~the~~ an edge of said first doped active layer.

18. (Previously presented) The diode according to claim 16, wherein said fourth doped active layer is an n-type region.

19. (Previously presented) The diode according to claim 16, wherein said fourth doped active layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

20. (Previously presented) The diode according to claim 9, further comprising a fourth doped active layer at least partially within said third doped active layer.

21. (Previously presented) The diode according to claim 20, wherein said fourth doped active layer is spaced away from the edge of said third doped active layer.

22. (Previously presented) The diode according to claim 20, wherein said fourth doped active layer is an n-type region.

23. (Previously presented) The diode according to claim 20, wherein said fourth doped active layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

24. (Original) The diode according to claim 1, wherein said diode is used in a CCD imager array.

25. (Original) The diode according to claim 1, wherein said diode is used in a CMOS imager array.

26. (Original) The diode according to claim 1, wherein said diode is used in a memory array.

27. (Original) The diode according to claim 1, wherein said diode is used in a logic device.

28. (Previously presented) A diode for use in an imaging device, said diode comprising:

an isolation region formed in a substrate;

a first doped active layer of a first conductivity type formed in said substrate, said substrate being of a second conductivity type, wherein said first doped active layer is spaced apart from said isolation region;

a second doped active layer of said first conductivity type formed within said first doped active layer, wherein said second doped active

layer is doped to a higher dopant dose than said first doped active layer, wherein said first active layer and said substrate form a p-n junction; and

a third doped region proximate to a lower boundary of said isolation region.

29. (Original) The diode according to claim 28, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

30. (Original) The diode according to claim 28, wherein said isolation region is a field oxide region formed by the Local Oxidation of Silicon.

31. (Original) The diode according to claim 28, wherein said isolation region is a field oxide region formed by the Shallow Trench Isolation process.

32. (Original) The diode according to claim 28, wherein said first doped active layer is spaced from said isolation region by from about 0.05 μm to about 1.0 μm.

33. (Original) The diode according to claim 28, wherein said first doped active layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

34. (Original) The diode according to claim 28, wherein said first doped active layer is spaced from said isolation region by about 0.2 μm to about 0.7 μm.

35. (Original) The diode according to claim 28, further comprising a first doped region of a second conductivity type under said isolation region.

36. (Original) The diode according to claim 35, wherein said first doped region is spaced away from the edge of said isolation region.

37. (Original) The diode according to claim 35, wherein said first doped region is a p-type region

38. (Original) The diode according to claim 28, wherein said first doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

39. (Original) The diode according to claim 38, wherein said first doped active layer is doped with phosphorous.

40. (Original) The diode according to claim 28, wherein said second doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

41. (Original) The diode according to claim 40, wherein said second doped active layer is doped with phosphorous.

42. (Original) The diode according to claim 28, wherein said first doped active layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm2 to about $1x10^{16}$ ions/cm^2.

43. (Original) The diode according to claim 28, wherein said second doped active layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

44. (Original) The diode according to claim 35, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

45. (Previously presented) The diode according to claim 28, wherein said first doped active layer is an n- region and said second doped active layer is an n+ region.

46. (Original) The diode according to claim 28, wherein said diode is used in a CCD imager array.

47. (Original) The diode according to claim 28, wherein said diode is used in a CMOS imager array.

48. (Original) The diode according to claim 28, wherein said diode is used in a memory array.

49. (Original) The diode according to claim 28, wherein said diode is used in a logic device.

50. (Previously presented) An imager device comprising:

(i) a processor; and

(ii) an imaging device coupled to said processor, said imaging device comprising:

a photodiode for use in said imaging device, said photodiode comprising:

an isolation region formed in a substrate;

a first doped photoactive layer of a first conductivity type formed in said substrate, wherein said first doped layer is spaced apart from said isolation region;

a second doped photoactive layer of a second conductivity type disposed in contact with said first doped photoactive layer, the contact of said first and second photoactive layers forming a p-n junction; and

a third doped region formed in said second doped photoactive layer beneath said isolation region.

51. (Original) The imager according to claim 50, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

52. (Original) The imager according to claim 50, wherein said isolation region is a field oxide region.

53. (Original) The imager according to claim 50, wherein said isolation region is a Shallow Trench Isolation region.

54. (Original) The imager according to claim 50, wherein said isolation region is formed of Local Oxidation of Silicon.

55. (Original) The imager according to claim 50, wherein said first doped photoactive layer is spaced from said isolation region by from about 0.05 μm to about 1.2 μm.

56. (Original) The imager according to claim 55, wherein said first doped photoactive layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

57. (Original) The imager according to claim 50, wherein said first doped photoactive layer is spaced from said isolation region by about 0.2 μm to about 0.7 μm.

58. (Original) The imager according to claim 50, further comprising a first doped region of a second conductivity type under said isolation region.

59. (Original) The diode according to claim 57, wherein said first doped region is spaced away from the edge of said isolation region.

60. (Original) The imager according to claim 58, wherein said first doped region is a p-type region.

61. (Original) The imager according to claim 50, wherein said first doped photoactive layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

62. (Original) The imager according to claim 67, wherein said first doped photoactive layer is doped with phosphorous.

63. (Original) The imager according to claim 67, wherein said first doped photoactive layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

64. (Original) The imager according to claim 58, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

65. (Original) The imager according to claim 50, wherein said imager is a CCD imager.

66. (Original) The imager according to claim 50, wherein said imager is a CMOS imager array.

67. (Previously presented) An imager device comprising:

(i) a processor; and

(ii) an imaging device coupled to said processor, said imaging device comprising:

a photodiode for use in an imaging device, said photodiode comprising:

an isolation region formed in a substrate;

a first doped photoactive layer of a first conductivity type formed in said substrate, said substrate being doped to a second conductivity type, wherein said first doped photoactive layer is spaced apart from said isolation region;

a second doped photoactive layer of said first conductivity type formed within said first doped photoactive layer, wherein said second doped photoactive layer is doped to a higher dopant dose than said first doped photoactive layer, wherein said first photoactive layer and said substrate form a p-n junction; and

a third doped region formed in said substrate beneath said isolation region and spaced apart from said first photoactive layer.

68. (Original) The imager according to claim 67, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

69. (Original) The imager according to claim 67, wherein said isolation region is a field oxide region.

70. (Previously presented) The imager according to claim 67 wherein said isolation region is a Shallow Trench Isolation region.

71. (Previously presented) The imager according to claim 67 wherein said isolation region is formed of Local Oxidation of Silicon.

72. (Original) The imager according to claim 67 wherein said first doped photoactive layer is spaced from said isolation region by from about 0.05 μm to about 1.2 μm.

73. (Previously presented) The imager according to claim 67 wherein said first doped photoactive layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

74. (Original) The imager according to claim 67 wherein said first doped photoactive layer is spaced from said isolation region by about 0.2 μm to about 0.7 μm.

75. (Original) The imager according to claim 67, further comprising a first doped region of a second conductivity type under said isolation region.

76. (Original) The imager according to claim 75, wherein said first doped region is spaced away from the edge of said isolation region.

77. (Original) The imager according to claim 75, wherein said first doped region is a p-type region.

78. (Original) The imager according to claim 67, wherein said first doped photoactive layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

79. (Original) The imager according to claim 78, wherein said first doped photoactive layer is doped with phosphorous.

80. (Original) The imager according to claim 67, wherein said second doped photoactive layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

81. (Original) The imager according to claim 80, wherein said second doped photoactive layer is doped with phosphorous.

82. (Original) The imager according to claim 80, wherein said first doped photoactive layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

83. (Original) The imager according to claim 82, wherein said second doped photoactive layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

84. (Original) The imager according to claim 77, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

85. (Previously presented) The imager according to claim 67, wherein said first doped photoactive layer is an n- region and said second doped photoactive layer is an n+ region.

86. (Original) The imager according to claim 67, wherein said imager is a CCD imager.

87. (Original) The imager according to claim 67, wherein said imager is a CMOS imager.

Claims 88-105 (Canceled).

106. (New) A diode, said diode comprising:

an isolation region formed in a substrate;

a first doped active layer of a first conductivity type formed in said substrate, wherein said doped active layer is spaced apart from said isolation region;

a second doped active layer of a second conductivity type in contact with said first doped active layer, the contact of said first and second active layers forming a p-n junction; and

a third doped region of said second conductivity type formed in said second doped active layer beneath said isolation region, wherein said third doped region is spaced away from an edge of said isolation region at a surface of said substrate.

107. (New) The diode according to claim 106, wherein said first doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

108. (New) The diode according to claim 107, wherein said first doped active layer is doped with phosphorous at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

109. (New) The diode according to claim 106, wherein said third doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

110. (New) The diode according to claim 106, further comprising a fourth doped active layer of said first conductivity type at least partially within said first doped active layer and having edges spaced away from edges of said first doped active layer.

111. (New) The diode according to claim 110, wherein said fourth doped active layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

112. (New) The diode according to claim 106, further comprising a fourth doped active layer of said first conductivity type at least partially within said third doped active layer and having edges spaced away from edges of said third doped active layer.

113. (New) The diode according to claim 106, wherein said diode is used in a memory device.

114. (New) The diode according to claim 106, wherein said diode is used in a logic device.